A High-Speed Cache Design

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Requirements and Goals

- Design an SRAM, including the schematic and layout, using FreePDK 45nm technology.
  - Capable of reading and writing one 32-bit word per clock cycle.
  - Robust enough to maintain operation with temperature, supply voltage, and process variability.
- Verify functionality through simulations.
- Optimize design to reduce key metric:

$$(\text{Energy per Access}) \times \text{Delay}^2 \times \text{Area} \times \text{IdlePower}$$

Key Parameters

Parameter	Value
Total Memory Size	64 kbit
Word Size	32 bit
# of Blocks	16
# of Columns/Block	64
# of Rows/Block	64
# of Words/Row	2

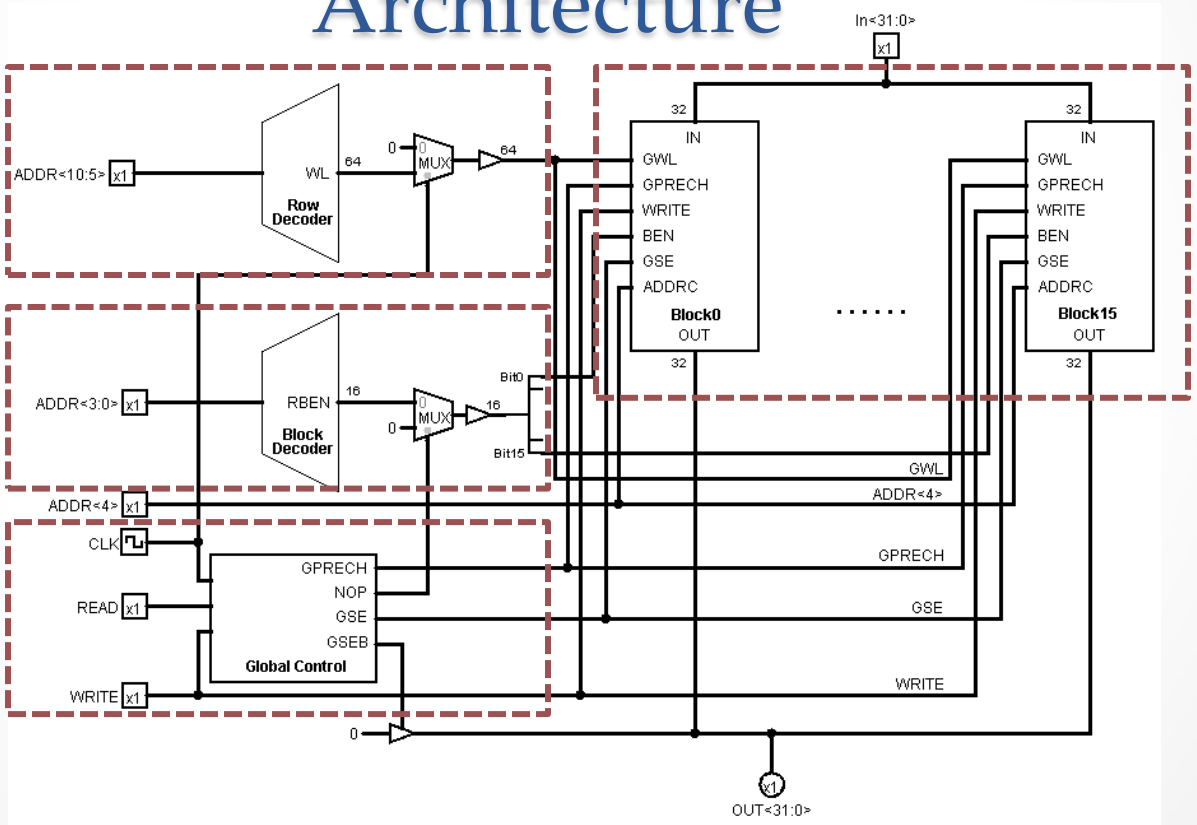
Architecture

Row Decoder

Block Decoder

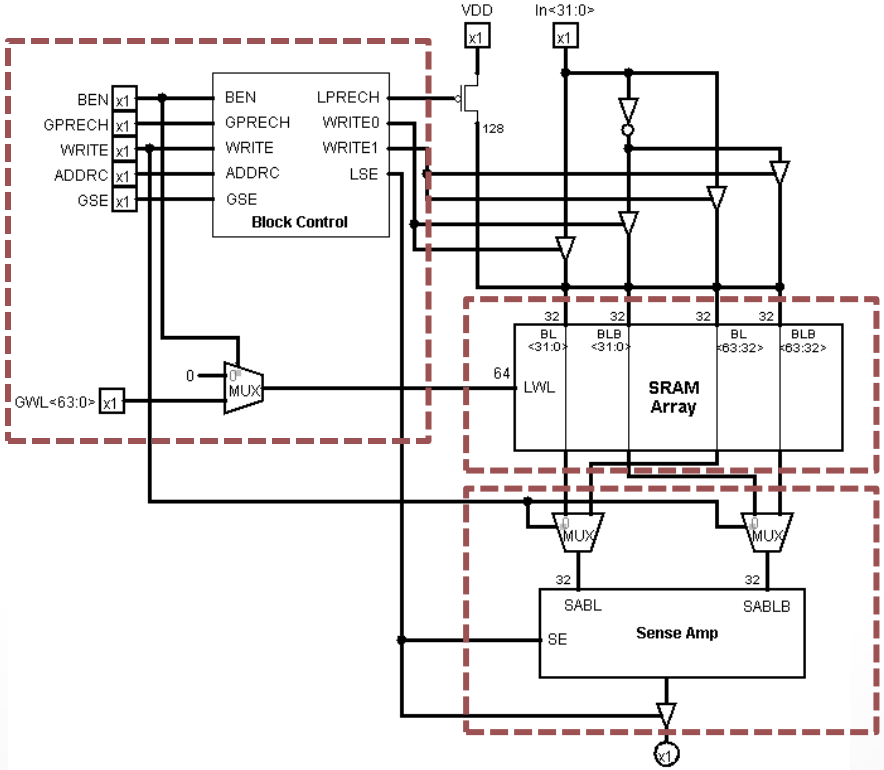
Control Block

Memory Blocks



Block Schematic

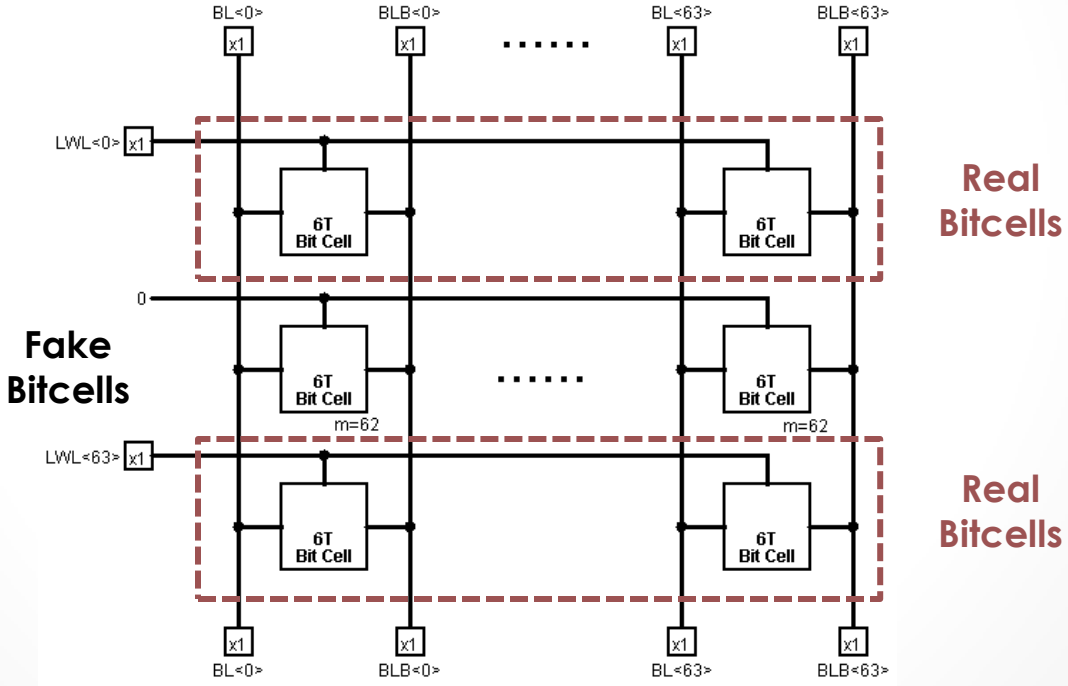
Control Block



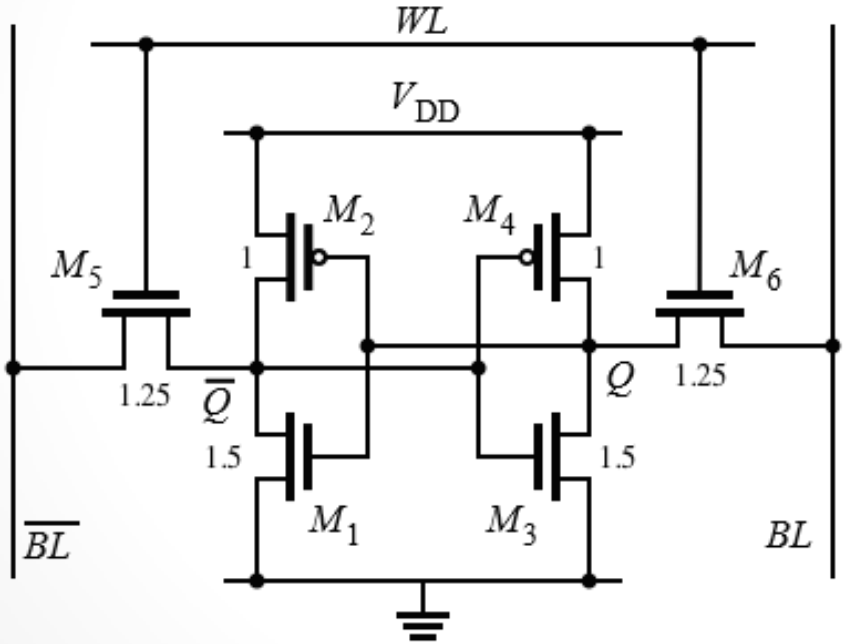
SRAM Array

Sense Amplifier

SRAM Array


BL<0>
BLB<0>
BL<63>
BLB<63>
x1
LWL<0>
6T
Bit Cell
Real
Bitcells
0
Fake
Bitcells
m=62
LWL<63>
Real
Bitcells

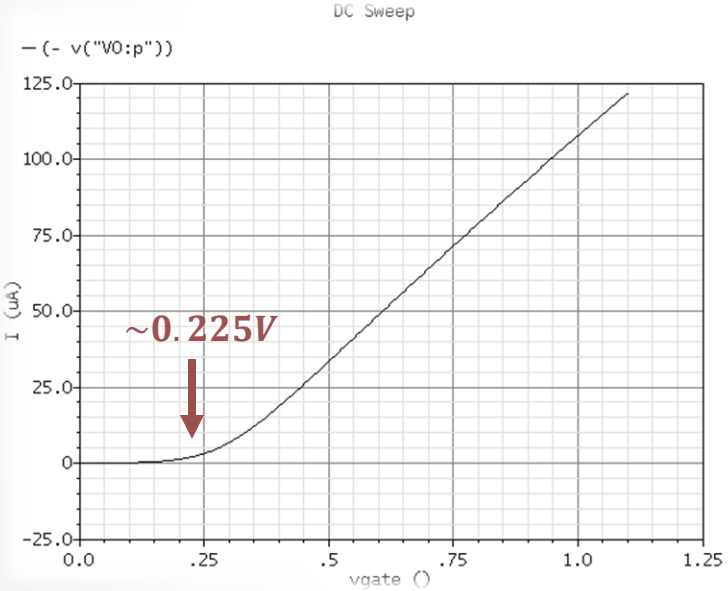
SRAM Bit Cell

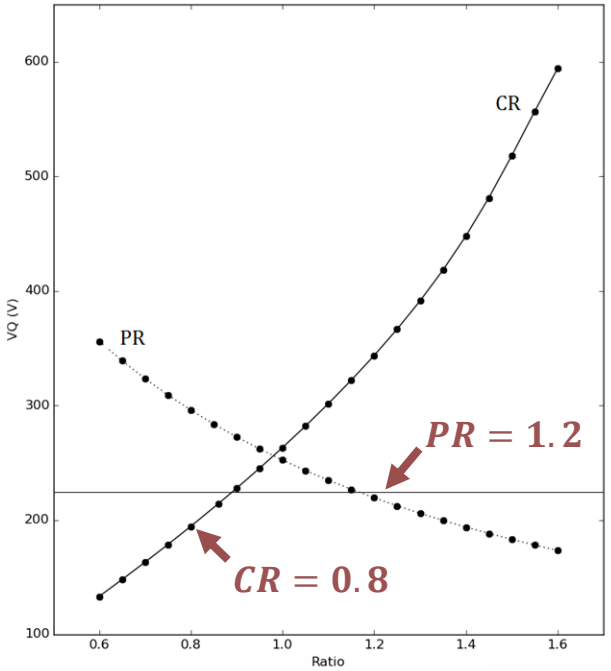


$$CR = \frac{W_1}{W_5} = \frac{W_3}{W_6} = 0.8$$

$$PR = \frac{W_2}{W_5} = \frac{W_4}{W_6} = 1.2$$

SRAM Bit Cell

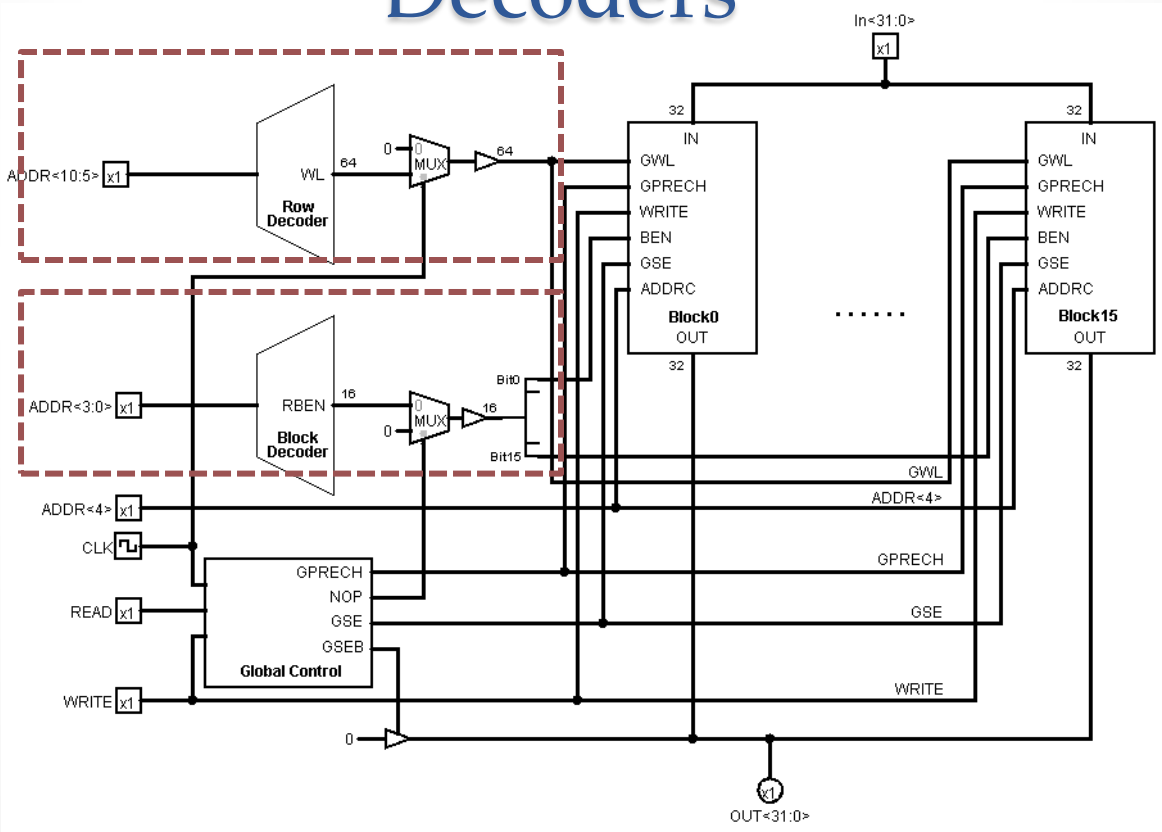




Decoders

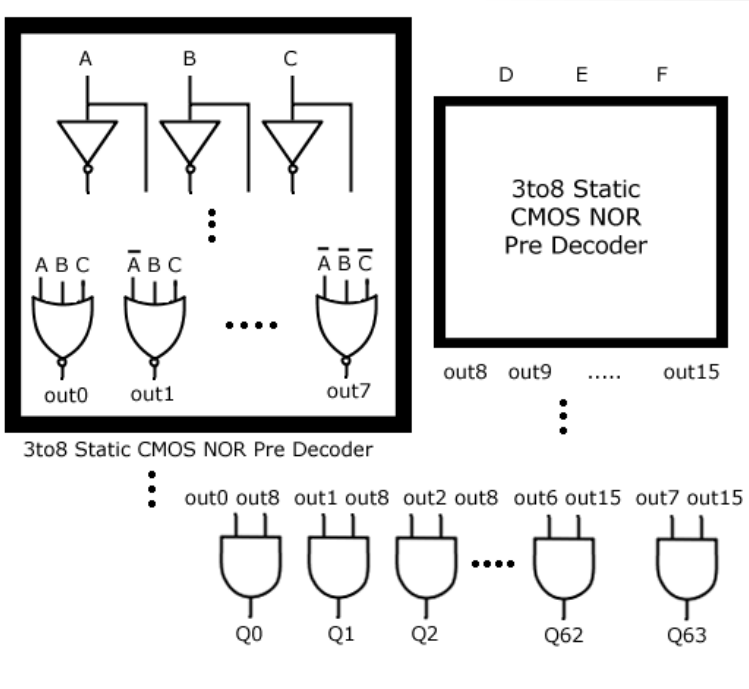
Row Decoder

Block Decoder



Row Decoder

- 6-to-64 decoder
- 2-stage hierarchy
  - predecoder stage
  - AND the outputs of 1st stage



Row Decoder - Comparing PreDec Architecture

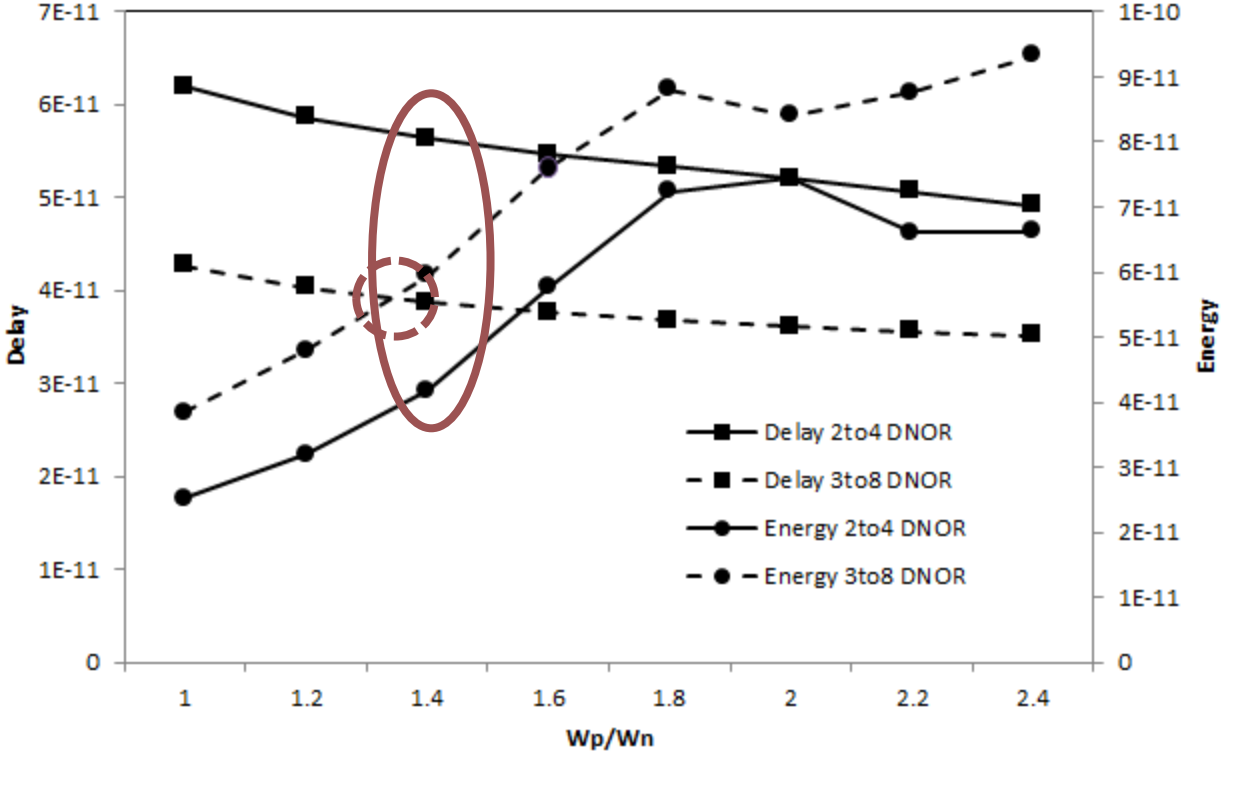
	Delay $D_0 \rightarrow Q_{63}$ (ps)	Energy (pJ)	# of FET
2-to-4 DNOR Pre Dec.	N/A	14.3	680
2-to-4 DNAND Pre Dec.	N/A	2.47	656
2-to-4 NOR Pre Dec.	102	0.715	572
2to4 NOR Pre Dec. with PMOS PG on Inverter	114	0.681	636
3-to-8 NOR Pre. Dec.	85.9	0.582	492

Row Decoder - Comparing 3-to-8 PreDec

3-to-8 NOR Pre Dec	Delay $D_0 \rightarrow Q_{63}$ (ps)	Energy (pJ)	# of FET
Original	85.9	0.582	492
PMOS PG on Inverter	95.5	0.553	556
PMOS PG on Inverter and HVT NMOS in NOR	88.0	0.592	556
Pass Gate (5 tran.) AND	112	0.684	556

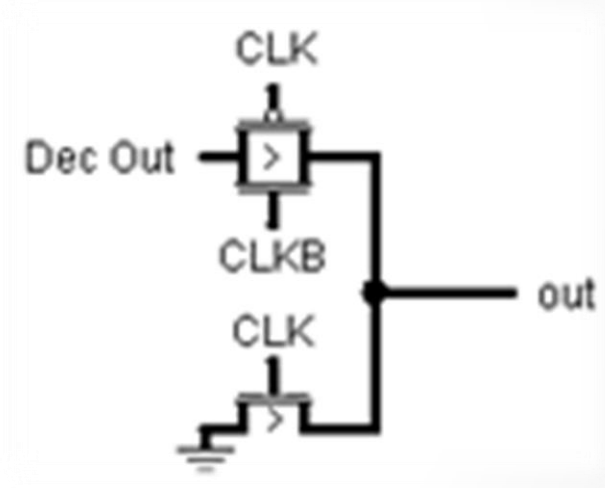
Row Decoder - Width

- The optimal widths (~1.4) are circled
- Still kept Wp/Wn at 1 to keep area and delay at minimum



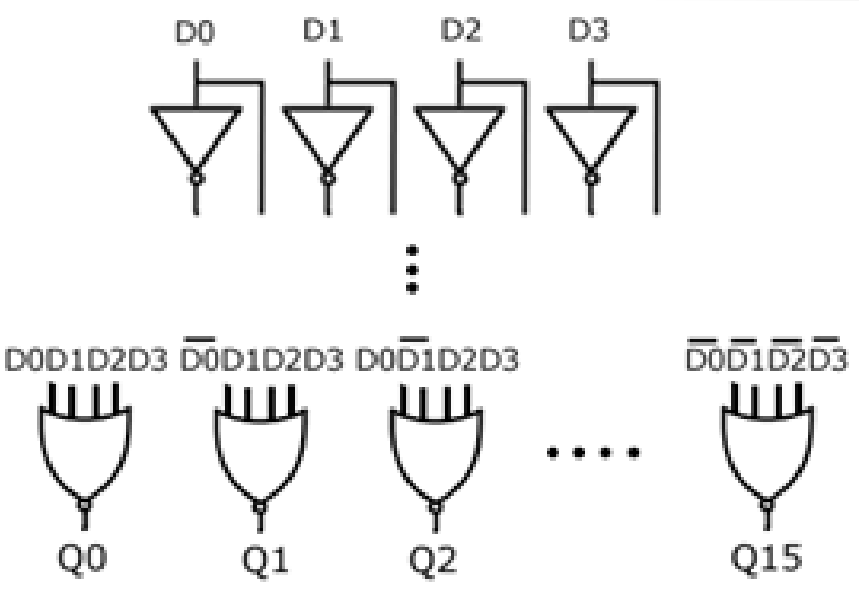
Row Decoder Output

- As long as decoder's delay is less than half a clock period, the delay for accessing the outputs is only 1 TX gate delay
- Transmission setup also drives outputs to 0 at the beginning



Block Decoder

- 4-to-16 Decoder



Block Decoder - Comparing Architectures

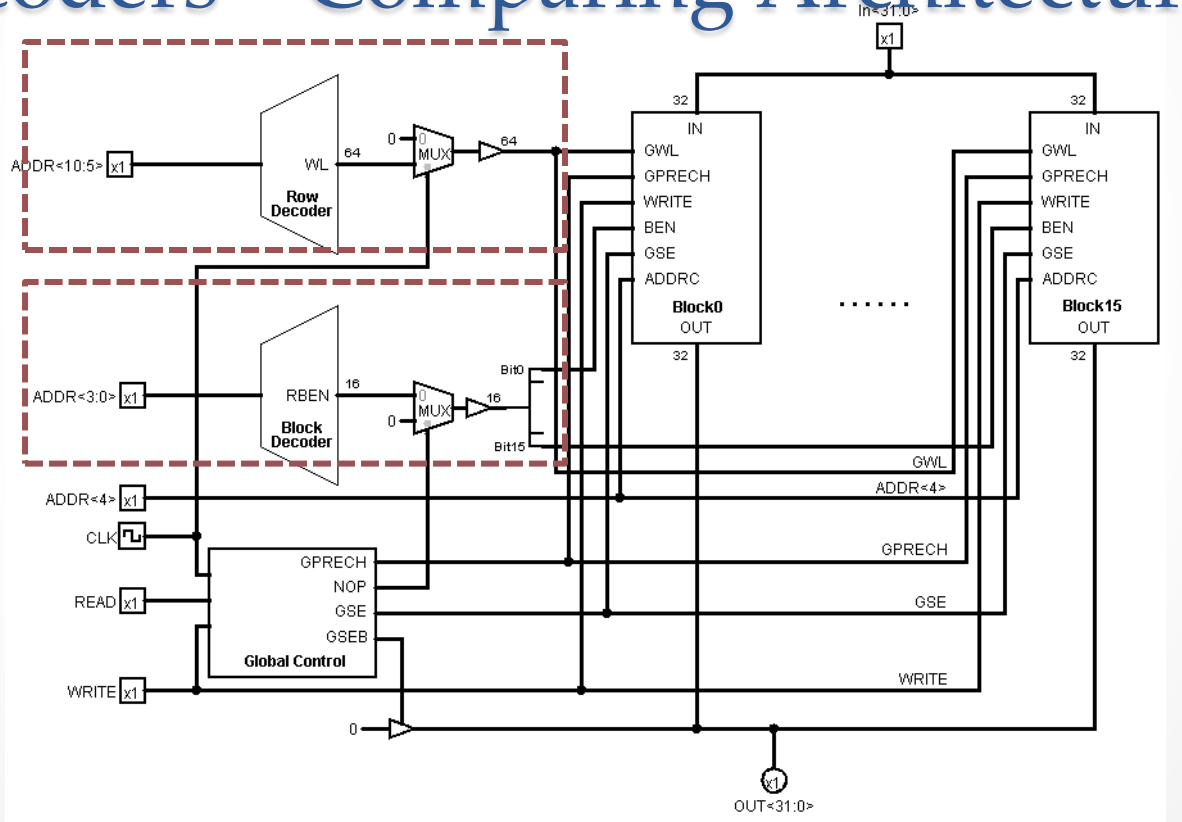
	Delay $D_0 \rightarrow Q_{63}$ (ps)	Energy (fJ)	# of FET
2-to-4 NOR Pre Dec.	47.5	96.3	136
2-to-4 NOR Pre Dec. with PMOS PG on Inverter	56.0	95.2	152
4to16 NOR	41.1	84.3	136

- Proven to be ~3ps faster in overall design than 4to16 NOR

Decoders – Comparing Architectures

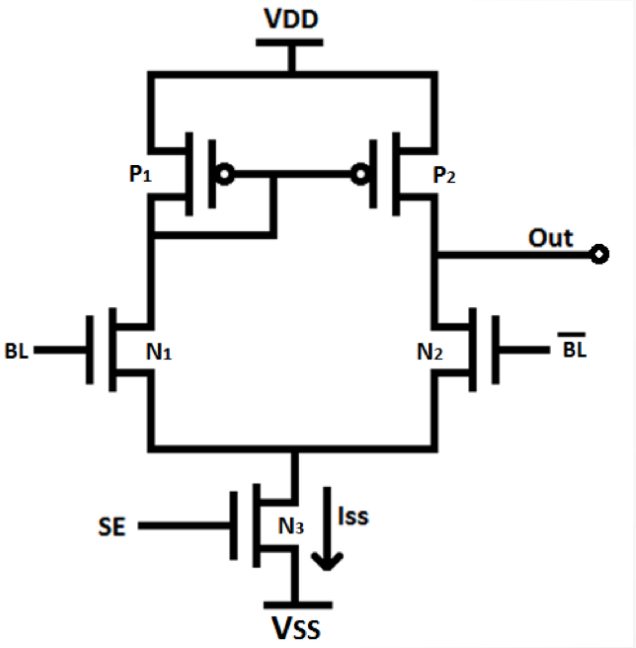
Row Decoder:
3-to-8 Static Nor PreDecoder

Block Decoder:
2-to-4 Static Nor PreDecoder

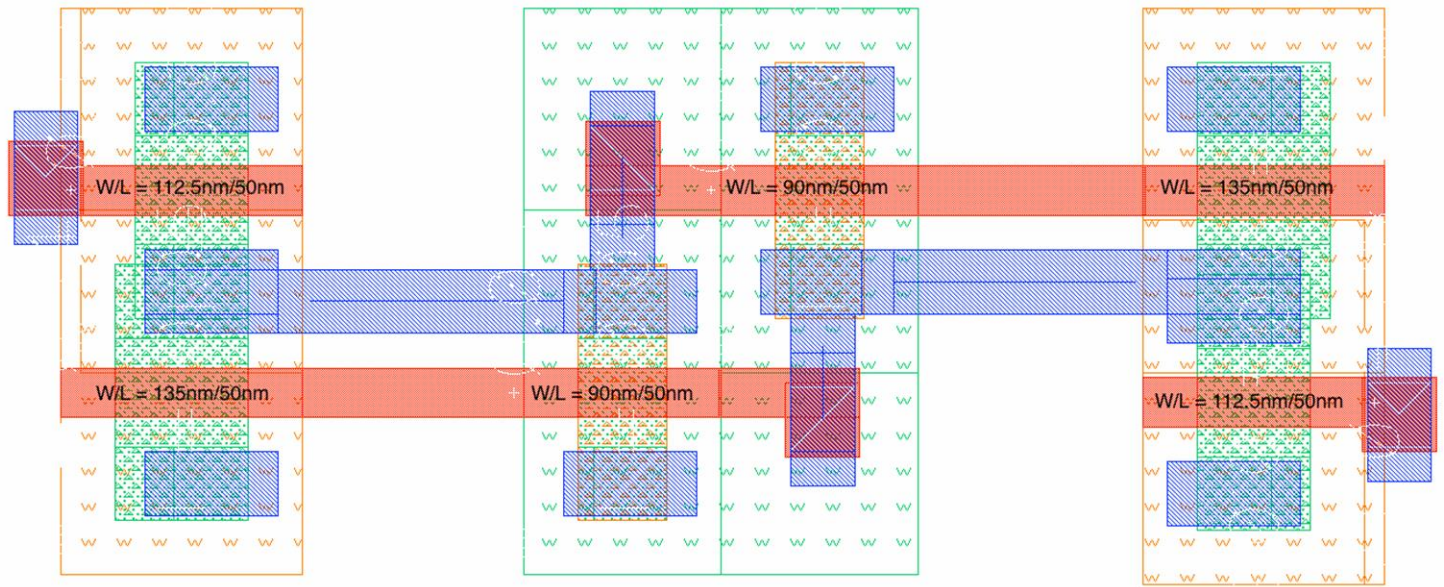


Sense Amplifier

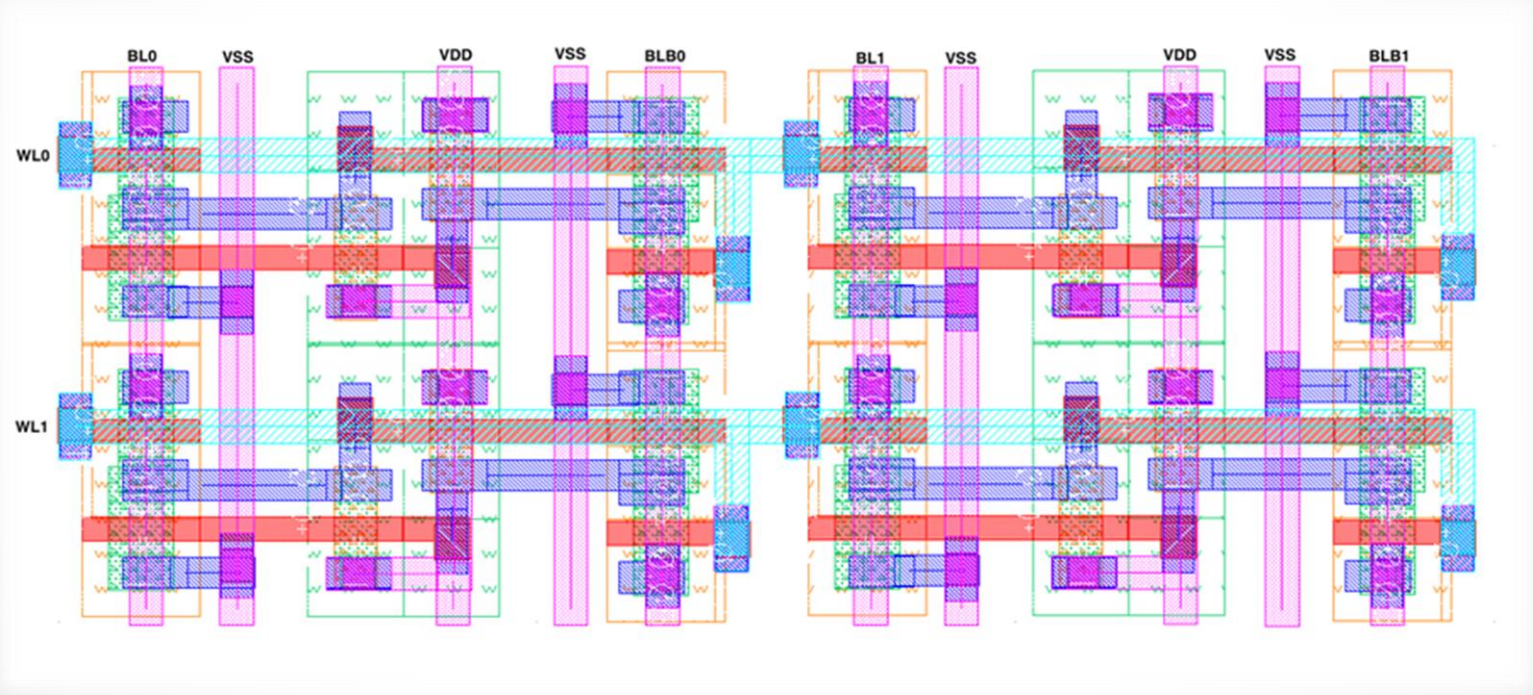
- voltage mode amplifier
- dynamic
- simple and reliable
- easy timing requirements
- resistant to supply noise variation



Bitcell Layout



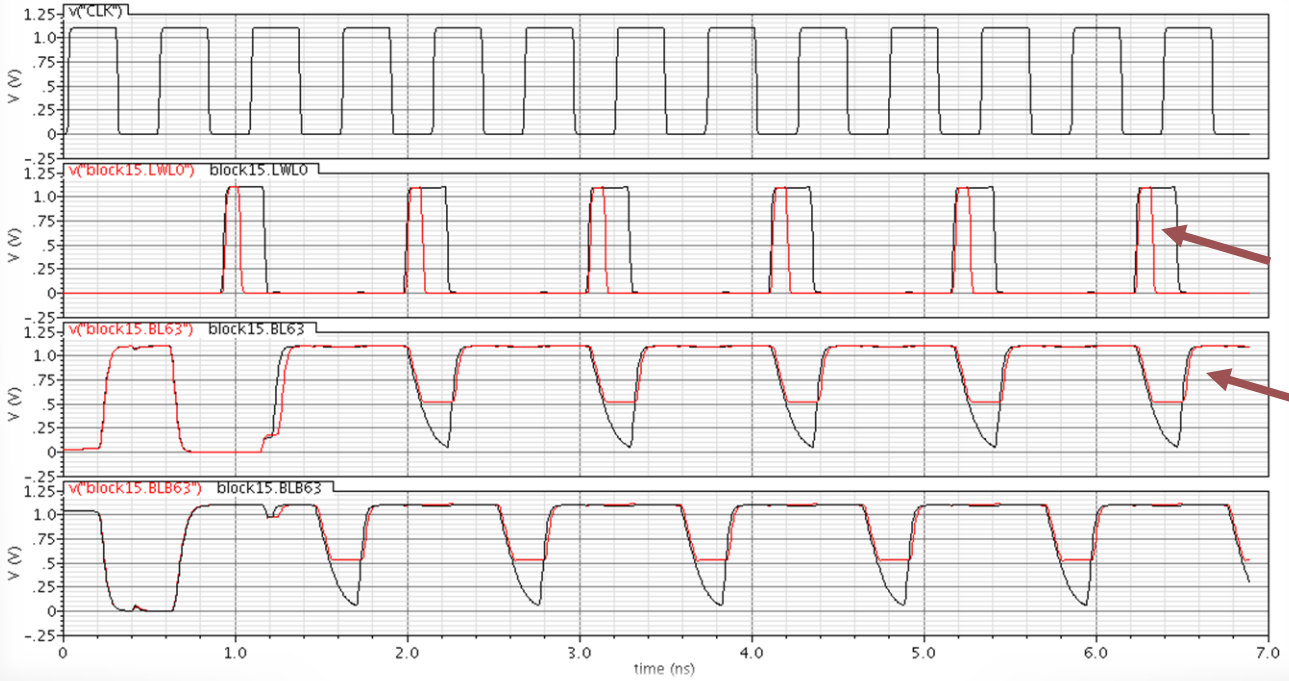
2-by-2 Bitcell Layout



Functionality

Energy Reduction

Energy Reduction



Metrics

Category	Metrics	Value
Delay	Read Delay	499 ps
	Write Delay	393 ps
	Minimum Clock Cycle	530 ps
Area	Bit Cell Area	0.71 μm^2
	Total Area (Estimate)	$> 0.105\ mm^2$
Energy	Energy Per Access	3.82 pJ
	Idle Power	2.43 mW
$(\text{Energy per Access}) \times \text{Delay}^2 \times \text{Area} \times \text{IdlePower}$		$3.09 \times 10^{-34}\ J\ sec^2\ mm\ W$